AF

PATENT

Docket No. Fuehrer 2-9-24-11

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTORS:	**T.E. Fuehrer** **K.E. Hollenbach** **D.R. Laturell** **S.B. Witmer**	EXAMINER: **R. SINGH**
APPLICATION NO.	**09/192,651**	GROUP ART UNIT: **2644**
FILED:	**November 16, 1998**	
TITLE:	**COMBINATION CLOCK AND CHARGE PUMP FOR LINE POWERED DAA**	

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service on October 6, 2004, in an envelope as First Class Mail, postage prepaid, addressed to: Commissioner for Patents, Mail Stop Appeal Brief - Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

10-6-04
Date

Lynn M. White
Lynn M.. White

Commissioner for Patents
Mail Stop Appeal Brief - Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANTS' BRIEF

This brief is in furtherance of the Notice of Appeal filed in this case on August 4, 2004.

This brief is transmitted in triplicate.

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1. REQUIRED FEE

A Credit Card Payment Form authorizing payment of the requisite fee ($340.00) set forth in §1.17(f) is enclosed. The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to Deposit Account No. 19-5425.

2. REAL PARTY IN INTEREST

The present application is assigned to **Agere Systems Guardian Corp.**, having its principal place of business at 555 Union Boulevard, Allentown, PA 18109. Accordingly, Agere Systems Guardian Corp. is the real party in interest.

3. RELATED APPEALS AND INTERFERENCES

The appellant, assignee, and the legal representatives of both are unaware of any other appeal or interference which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

4. STATUS OF CLAIMS

A. Claims canceled: 14 and 17

B. Claims withdrawn from consideration but not canceled: None

C. Claims pending: 1-13, 15-16, and 18-19

D. Claims allowed: None

E. Claims rejected: 1-13, 15-16, and 18-19

F. Claims appealed: 1-13, 15-16, and 18-19

Appealed claims 1-13, 15-16, and 18-19 as currently pending are attached as Appendix A hereto.

5. STATUS OF AMENDMENTS

No amendments after final (37 C.F.R. 1.116) were made in the application. No amendments were made in a Reply under 37 C.F.R. §§1.112 filed on December 19, 2003 which resulted in the final Office Action appealed herein. In a previous Reply, filed May 6, 2003, claims 1, 5, 7, 8, 10, and 12 were amended.

6. SUMMARY OF THE CLAIMED INVENTION

The present invention relates to an interface utilizing existing clock signals from a driver circuit, such as a DSP, to charge capacitors that are normally used for capacitive coupling of digital data across a high voltage isolation barrier. A clock regeneration circuit is included to regenerate the clock signals used to charge the capacitors, thereby effectively preserving the integrity of the clock so that it can be used, for example, to generate a timing event.

Using relatively small capacitors (e.g., capacitors in the range between 10 pF and 500 pF, and preferably at 100 pF) a charge pump is formed to generate power to the interface at all times. Thus, the interface always has a steady source of power available for use, including during the on-hook state, for powering circuitry that can detect, modulate, and transmit on-

hook signals across the capacitive interface, and also has a clock available for timing events as described above.

The claimed invention includes circuitry that doubles the voltage of the clock signal coming from the DSP, thereby obtaining more power for use by a data access arrangement (DAA) coupled to the interface and, therefore to the DSP. Further, the interface circuit is a fully differential circuit, thereby eliminating the need to keep the impedance across the capacitive coupling low, as is required when using a pseudo-differential interface circuit.

7. ISSUES

A. 35 U.S.C. §103 ISSUES INVOLVING CLAIMS 1-13, 15-16, and 18-19

1. Whether the Examiner improperly rejected the claims under 35 USC §103 because the cited prior art fails to present a reason, suggestion, or motivation to combine Scott et al. and Luscher, Jr. to obtain a driver circuit, such as a charge pump, which doubles the voltage of a clock signal provided by the driver circuit to thus increase the voltage available for use by a DAA and regenerate the clock signal so that it is also available to perform its clocking function.

8. GROUPING OF CLAIMS

A. Claims 1-13, 15, 16, 18 and 19 stand or fall together.

9. ARGUMENT

A. The Claimed Invention Is Not Taught or Suggested by Scott or Luscher, Either Alone or in Combination

1. Scott et al., U.S. Patent No. US 6,385,235 B1

U.S. Patent No. 6,385,235 to Scott et al. teaches an isolation system suitable for use in telephony. In a preferred embodiment of Scott, a capacitive isolation barrier across which a digital signal is communicated is provided. The isolation barrier comprises two high voltage capacitors. In a preferred embodiment, a clock recovery circuit is connected to the isolation capacitors. The clock recovery circuit recovers a clock signal from the digital data driven across the isolation barrier and provides a synchronized clock signal to the various circuits in the received system.

2. Luscher, Jr., U.S. Patent No. 5,600,551

U.S. Patent No. 5,600,551 to Luscher, Jr. teaches a voltage multiplier and capacitive isolation power supply using capacitors, diodes and first and second clock signals that are out of phase with respect to each other. When the first clock signal is high and the second clock signal is low, a capacitor in a first stage transfers charge to a capacitor in a second stage. When the first clock signal is low and the second clock signal is high, the capacitor in the second stage transfers charge to an output capacitor, and the capacitor in the first stage is recharged via a feedback diode between a capacitor connected to a ground potential and the

capacitor in the first stage. Additionally, the capacitors in each of the stages provide an isolation function for the power supply.

To support a rejection under 35 U.S.C. §103, the cited references must provide a reason, suggestion, or motivation to lead an inventor to combine two or more references.

> "To prevent the use of hindsight based on the invention to defeat patentability of the invention, this Court [the Federal Circuit] requires the Examiner to show a motivation to combine the references that create the case of obviousness. In other words, the Examiner must show reasons that the skilled artisan, **confronted with the same problems as the inventor** and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed."

In re Rouffet, 149 F.3d 1350, 47 U.S.P.Q. 2d 1453 (Fed.Cir. 1998) (emphasis added).

Neither of the references cited by the Examiner teach or suggest a driver circuit, such as a charge pump, which doubles the voltage of a clock signal provided by the driver circuit to thus increase the voltage available for use by a DAA and regenerates the clock signal so that it is also available to perform its clocking function.

The mere finding of a teaching of doubling the voltage of a clock signal is not, in itself, enough to suggest the present claimed invention. Nowhere does the Examiner point to any motivation to combine the references to achieve the claimed invention. Nothing indicates that either Scott or Luscher had any concern about needing a high voltage to operate a DAA than the clock voltage, i.e., there is nothing to indicate that either of them were confronted with the same problems as the Applicant herein.

Applicant was motivated to provide the voltage doubling because they were using a three volt process and needed to have the higher voltage to be used by the DAA coupled to the interface and, therefore, to the DSP. The Examiner provides no evidence of motivation in either reference indicating the desirability, need, etc. for doubling the clock voltage in view of the use of a 3 volt process. Without such a suggestion, the mere existence of a patent allegedly teaching doubling the voltage of a clock signal for a different reason does not rise to the level required under 35 U.S.C. §103 for a finding of obviousness. The Examiner has merely used impermissible hindsight to make the present rejection.

The claims of the present invention, as amended, positively recite these novel and distinguishing features (claim 1, "A fully differential interface circuit ... having a clock generator generating a clock signal ... a clock regeneration element ... said clock regeneration element regenerating a clock signal that is essentially identical to the clock signal generated by said clock generator"; claim 7, "A method of providing power to a data access arrangement in an interface circuit ... said method comprising the steps of ... generating a power signal ... across said charge pump by inputting the output of said clock generator to said charge pump ... regenerating a clock signal essentially identical to said output of said clock generator"; claim 8, "A fully differential interface circuit ... a driver circuit ... said driver circuit including a clock generator generating a clock signal ... a clock regeneration element ... said clock regeneration element regenerating a clock signal that is essentially identical to the clock signal generated by the clock generator"). Since these claimed elements are neither taught nor

suggested by either Scott or Luscher, it is submitted that the claims, as amended, patentably define over the cited references.

The present invention patentably defines over the cited references and is thus in condition for allowance. The Board is thus respectfully requested to reconsider and overrule the Examiner's rejection of the claims under 35 U.S.C. §103.

10. CONCLUSION

For the foregoing reasons applicants respectfully request this Board to overrule the Examiner's rejections and allow claims 1-13, 15-16, and 18-19.

Respectfully submitted:

10/6/04
Date

Mark D. Simpson
Registration No. 32,942

Synnestvedt & Lechner LLP
2600 Aramark Tower
1101 Market Street
Philadelphia, PA 19107
Telephone: 215-923-4466
Facsimile: 215-923-2189

APPENDIX A

CLAIMS INVOLVED IN THIS APPEAL:

1. (Previously presented) A fully differential interface circuit, comprising:

a digital signal processor (DSP) having a clock generator generating a clock signal having a voltage;

a data access arrangement (DAA) having a clock regeneration element; and

a charge pump, coupled between said DSP and said DAA, said charge pump providing operating power to said DAA, said charge pump doubling the voltage of said clock signal, and said clock regeneration element regenerating a clock signal that is essentially identical to the clock signal generated by said clock generator.

2. (Previously presented) An interface circuit as set forth in claim 1, wherein said charge pump comprises:

a first capacitive element having an input side connected to said DSP and an output side connected to said DAA;

a second capacitive element having an input and an output each connected to said DAA; and

a rectifying element coupled between the output side of said first capacitive element and said second capacitive element, said rectifying element receiving said clock signal from said DSP and doubling the voltage of said clock signal before passing said clock signal to said DAA.

3. (Original) An interface circuit as set forth in claim 2, wherein said DSP includes a clock generator generating first and second clock pulses out of phase with each other by 180° and wherein said first capacitive element comprises:

a first capacitor coupled to receive said first clock pulse; and

a second capacitor coupled to receive said second clock pulse, wherein said first capacitive element continuously outputs a positive output voltage to said rectifying element.

4. (Original) An interface circuit as set forth in claim 3, wherein said rectifying element comprises a diode rectifier.

5. (Previously presented) An interface circuit as set forth in claim 4, wherein said clock regeneration element is connected in parallel with said rectifying circuit to remove DC level shift and regenerate ~~a~~ clock pulses for use by the DAA which are essentially identical to the clock pulses output by said clock generator.

6. (Original) An interface circuit as set forth in claim 5, wherein said second capacitive element comprises a storage capacitor which stores the charge transferred by said first and said second capacitors.

7. (Previously presented) A method of providing power to a data access arrangement (DAA) in an interface circuit of a telecommunication network when a telephone line connected to said interface circuit is in the on-hook state, said interface circuit including a digital signal processor (DSP) having a clock generator, said method comprising the steps of:

inserting a charge pump between said DSP and said DAA;

generating a power signal, having a voltage, across said charge pump by inputting the output of said clock generator to said charge pump;

doubling the voltage of said power signal and storing said generated power signal for use by said interface; and

regenerating a clock signal essentially identical to said output of said clock generator.

8. (Previously presented) A fully differential interface circuit, comprising:

a driver circuit for developing a charge across capacitive elements of said interface circuit, said charge having a voltage, said driver circuit including a clock generator generating a clock signal;

a data access arrangement (DAA) having a clock regeneration element; and

a charge pump, coupled between said DAA and said driver circuit, said charge pump providing operating power to said DAA, said charge pump doubling the voltage of said charge and passing said doubled voltage to said DAA to provide said operating power, and said clock regeneration element regenerating a clock signal that is essentially identical to the clock signal generated by said clock generator.

9. (Previously presented) An interface circuit as set forth in claim 8, wherein said charge pump comprises:

a first capacitive element having an input side connected to said driver circuit and an output side connected to said DAA;

a second capacitive element having an input and an output each connected to said DAA; and

a rectifying element coupled between the output side of said first capacitive element and said second capacitive element, said rectifying element receiving said charge from said driver circuit and doubling the voltage of said charge before passing said charge to said DAA.

10. (Previously presented) An interface circuit as set forth in claim 9, wherein said clock signal generated by said clock generator comprises first and second clock pulses out of phase with each other by 180° and wherein said first capacitive element comprises:

a first capacitor coupled to receive said first clock pulse; and

a second capacitor coupled to receive said second clock pulse, wherein said first capacitive element continuously outputs a positive output voltage to said rectifying element.

11. (Original) An interface circuit as set forth in claim 10, wherein said rectifying element comprises a diode rectifier.

12. (Previously presented) An interface circuit as set forth in claim 11, wherein said clock regeneration element is connected in parallel with said rectifying circuit to remove DC level shift and regenerate a clock pulses for use by the DAA which are essentially identical to the clock pulses output by said clock generator.

13. (Original) An interface circuit as set forth in claim 12, wherein said second capacitive element comprises a storage capacitor which stores the charge transferred by said first and said second capacitors.

14. (Cancelled)

15. (Previously presented) An interface circuit as set forth in claim 2, wherein said first capacitive element has a capacitance sufficient to create said charge pump.

16. (Previously added) An interface circuit as set forth in claim 2, wherein the first capacitive element has a capacitance value of approximately 100 pF.

17. (Cancelled)

18. (Previously presented) An interface circuit as set forth in claim 9, wherein said first capacitive element has a capacitance sufficient to create said charge pump.

19. (Previously added) An interface circuit as set forth in claim 9, wherein the first capacitive element has a capacitance value of approximately 100 pF.